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***EC34XX Digital Logic and Computer Organization***

**L-T-P-Cr: 3-0-0-3**

**Pre-requisites:** Elements of Electronics Engineering

**Objectives/Overview:**

* This course is intended to provide the students with a good knowledge of all varieties of Digital Circuits (both combinational & sequential circuits) & timing circuits, IC Chips, their design & applications along with Analog to Digital & Digital to Analog conversion of Signals.
* The students are also exposed to different types of RAMs & ROMs with their in depth knowledge.

**Course Outcomes:**

At the end of the course, a student should be able to:

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| **Sl. No.** | **Outcome** | **Mapping to POs** |
|  | Design & implement digital circuits using logic gates IC chips | PO4, PO2 |
|  | Design & implement digital circuits using multiplexer & demultiplexer IC chips. | PO1, PO2 |
|  | Design & implement registers & counters using different flip-flop IC chips. | PO2 , PO3 |
|  | Familiarization with basic organizational units of computer | PO4, PO3 |

**UNIT I: Minimization Technique and Logic Gates Lectures: 5**

Number Systems, Boolean postulates and laws, De- Morgan’s Theorem, Principle of Duality Boolean expression, Minimization of Boolean expressions, Minterm, Maxterm, SOP, POS, Karnaugh map Minimization, Don’t care conditions, Quine Mc Cluskey method of min-imization. Binary Codes: Gray Code, BCD Code. Logic Gates: AND, OR, NOT, NAND, NOR, Exclusive OR and Exclusive NOR. Implementations of Logic Functions using gates, NAND–NOR implementations, Multi level gate implementations.

**UNIT II: Analysis and Synthesis of Combinatorial Logic Circuits Lectures: 6**

Adders and Subtractors, Carry look-ahead adders; Multiplexers; De-multiplexers; Encoders; Priority Encoder; Decoders; Code Converters; Magnitude Comparators; Parity generators and Checkers

**UNIT III: Sequential Circuits Lectures: 9**

Sequential Circuit Blocks-Latches, Flip Flops- Race around condition, Master-Slave and edge triggered SR, JK, D & T Flip Flop; Shift Registers; Counters- Synchronous and synchronous, design of ripple counter. Johnson counter, ring counter, sequence generator, Finite state machine (Mealy and Moore Type)

**UNIT IV:** **Lectures: 10**

**Computer Arithmetic & ALU:** Structural and functional views of computer system; ALU and data path. Computer arithmetic; ALU data path design for integer addition, subtraction, multiplication and division; Fixed-point and floating-point representations; FPU data path design for floating-point addition, subtraction, multiplication and division; Guard, round and sticky bits in FPU.

**UNIT V:** **Lectures: 12**

**Memory System**: Memory system characteristics and design objectives; Memory hierarchy in CISC and RISC systems; Cache memory principle and organization; Cache memory mapping; Cache replacement algorithms; Cache writing policies; Unified and split caches; Random access memory; External memory: disk-based storage and RAIDs, optical storage, SSD storage; Virtual memory, paging and segmentation.

**Input/Output Organization:** I/O structures and functions; I/O techniques: programmed I/O, interrupt-driven I/O, DMA; Interrupt and interrupt controller; Bus arbitration.

**Text/Reference Books**

1. *Digital Systems- Principles & Applications.* Tocci, Widmar and Jain, Pearsons
2. *Digital Fundamentals.* Floyd and Jain, Pearson
3. *Digital Circuits (Vol-I & vol-II).* D. Roychowdhary, Platinum Publishers.
4. *Fundamentals of VHDL Design.* Stephen Brown and Zovenkeo Vrasesic, TMH
5. *Introduction to Logic Design with CDROM.* Alan B. Marcovity, TMH
6. *Fundamentals of Digital Logic with Verilog Design.* Stephen Brown, TMH
7. *Modern Digital Electronics.* R. P. Jain, TMH.
8. *Problems and solution on Digital circuits (Vol-I & Vol-II).* D. Roychowdhary, Platinum Publishers.
9. Andrew S. Tanenbaum, Todd Austin, *Structured Computer Organization*, Pearson Education, Sixth edition, 2013.